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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/517,308	DE SMET ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37,39,44-47,50-52,54 and 56-65* is/are rejected.

7)☒ Claim(s) *38,40-43,48,49,53,55 and 66* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 12-22-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 32-33,46-47,50-52,54,56-59,61-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKnight (US Patent No. 6,304,239 B1).

As to claim 32, McKnight teaches an array of pixels (See Col. 1, Lines 18-24), each pixel comprising:

a pixel element, each pixel element comprising a first pixel electrode for individual control of the pixel element and a second pixel electrode, the second pixel electrode linking substantially all pixel elements in the array and being connected to a common counter-electrode, the first and second pixel electrode forming a first capacitor, the pixel element having a modulation voltage (in the reference is equivalent to pixel electrode voltage) (See Fig. 1A, items 26,28, from Col. 6, Line 59 to Col 7, Line 27),

a pixel refresh circuit, for transferring electric charge related to a pixel data value from a data input of the pixel to the first pixel electrode via a charge transfer path (See Fig. 2A, items 102,104),

a first memory element coupled to the pixel data input for storing electric charge related to the pixel data value (See Fig. 6C, item 673),

a first switch element located between the first memory element and the first pixel electrode for controlling charge transfer from the first memory element through the charge transfer path to the first pixel electrode (See Fig. 6C, item 674, Col. 12, Lines 39-52),

wherein the first switch element and the first memory element co-operate to transfer charge related to the pixel data value passively along the charge transfer path to the first capacitor (See Fig. 6C, items 673-674, Col. 12, Lines 39-52) and wherein the array further comprises means for applying a dynamically changing voltage to the common counter-electrode (See Fig. 17, items Vmin, Vmax, 1704, Col. 25, Lines 28-40), the dynamically changing voltage changing between minus the voltage of the pixel elements (See Fig. 17, item Vmin) and the sum of the voltage and the modulation voltage of the pixel elements (See Fig. 17, item Vmax) so that the pixel data value is a signal comprised between zero volts and a data voltage value (See Fig. 17, item 1702), the data voltage value being not smaller than the modulation voltage (in the reference the data voltage value being is equal to the modulation voltage) (See Fig. 17, item 1702) and smaller than the sum of the modulation voltage and the voltage of any of the pixel elements (See Fig. 17, Pixel Electrode Voltage < Velectro-optic, from Col. 25, Line 27 to Col. 26, Line 5).

McKnight does not disclose a threshold voltage of the pixel element.

McKnight teaches the voltage between Vmin, Vmax and Pixel Electrode Voltage (See Fig. 17).

It would have been obvious to one ordinary skill in the art at the time of invention to use threshold voltage of the pixel element (for example TFT) as difference between Vmin, Vmax and Pixel Electrode Voltage in order to use higher threshold for LC material than for the driving circuit (See Col. 4, Lines 25-36 in McKnight reference).

As to claims 33,46 McKnight teaches the first memory element having a first and a second electrode, the first electrode being coupled to the pixel data input, wherein the second electrode is coupled to ground (See Fig. 6C, item 673, Col. 12, Lines 39-52).

As to claims 50-51 McKnight teaches the pixel element is a liquid crystal (See Col. 1, Lines 17-24 and Col. 4, Lines 25-36).

As to claims 52,54,56 McKnight teaches a storage capacitor, transistor and active matrix (See Fig. 6C, items 673-674,Col. 12, Lines 39-52).

As to claim 57, McKnight teaches a method for refreshing pixel values of an array of pixels (See Col. 1, Lines 18-24), each pixel comprising: a pixel element, each pixel element comprising a first pixel electrode for individual control of the pixel element and a second pixel electrode, the second pixel electrode linking substantially all pixel elements in the array and being connected to a common counter-electrode, the first and second pixel electrode forming a first capacitor, the pixel element having a modulation voltage (in the reference is equivalent to pixel electrode voltage) (See Fig. 1A, items 26,28, from Col. 6, Line 59 to Col 7, Line 27), method comprising passively transferring charge related to the pixel data value passively along the charge transfer path to the first capacitor (See Fig. 6C, items 673-674, Col. 12, Lines 39-52) and applying a

dynamically changing voltage to the common counter-electrode (See Fig. 17, items Vmin, Vmax, 1704, Col. 25, Lines 28-40), the dynamically changing voltage changing between minus the voltage of the pixel elements (See Fig. 17, item Vmin) and the sum of the voltage and the modulation voltage of the pixel elements (See Fig. 17, item Vmax) so that the pixel data value is a signal comprised between zero volts and a data voltage value (See Fig. 17, item 1702), the data voltage value being not smaller than the modulation voltage (in the reference the data voltage value being is equal to the modulation voltage) (See Fig. 17, item 1702) and smaller than the sum of the modulation voltage and the voltage of any of the pixel elements (See Fig. 17, Pixel Electrode Voltage < Velectro-optic, from Col. 25, Line 27 to Col. 26, Line 5).

McKnight does not disclose a threshold voltage of the pixel element.

McKnight teaches the voltage between Vmin, Vmax and Pixel Electrode Voltage (See Fig. 17).

It would have been obvious to one ordinary skill in the art at the time of invention to use threshold voltage of the pixel element (for example TFT) as difference between Vmin, Vmax and Pixel Electrode Voltage in order to use higher threshold for LC material than for the driving circuit (See Col. 4, Lines 25-36 in McKnight reference).

As to claims 58-59, McKnight teaches before transferring the charge related to pixel data, storing the charge related to pixel data (See Fig. 6C, item 673).

As to claims 61-63, McKnight teaches the transferring is synchronized with the applied dynamically changing voltage to the common counter-electrode, pulsing light sources with different colors, wherein pulsing a light source

with a new color is synchronized with the transferring (See Figs. 3A-3B, items 202-228, from Col. 9, Line 38 to Col. 10, Line 59).

As to claim 64, McKnight teaches storing charge related to complementary pixel data (See Fig. 17, items Negative Frame time, Positive Frame Time, from Col. 25, Line 41 to Col. 26, Line 5).

As to claims 47, 65 McKnight teaches the step of passively transferring pixel data comprises losslessly mirroring the data from a first memory element to the first pixel electrode of the pixel element (See Fig. 6C, items 671-673, Col. 12, Lines 39-52).

3. Claims 34-35,44-45,60 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKnight as applied to claim 32,58 above, and further in view of Willis et al. (US Patent No. 7,038,671 B2).

As to claims 34,60 McKnight does not disclose each pixel further comprises conversion means for converting a stored amount of electric charge related to the pixel data value into a pulse with a pulse width for control of the pixel element, the pulse width corresponding to the stored amount of electric charge.

Willis et al. teaches each pixel further comprises conversion means for converting a stored amount of electric charge related to the pixel data value into a pulse with a pulse width for control of the pixel element, the pulse width corresponding to the stored amount of electric charge See Fig. 1, item 37b, Col. 3, lines 21-410.

It would have been obvious to one ordinary skill in the art at the time of invention to incorporate teachings of Willis et al. into McKnight system in order to drive an SLM device (See Col. 1, Lines 58-59).

As to claims 35,44 Willis teaches a comparator device (See Fig. 2, item 142).

As to claim 45, it generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent of showing criticality of in a particular recited value. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to interchange number of transistors. Such a limitation would have been considered as obvious variation on the matter of number transistors over the prior art of McKnight and Willis et al. In re Rose, 105 USPQ 237 (CCPA 1955).

4. Claims 36-37 rejected under 35 U.S.C. 103(a) as being unpatentable over Willis et al. and McKnight as applied to claim 35 above, and further in view of Kusumoto et al. (US Patent No. 5,402,128).

As to claim 36-37,39 Willis et al. and McKnight do not disclose the comparator device comprises a switching circuit (resistive load inverter) and wave-shaping circuit (inverter).

Kusumoto et al. teaches the comparator device comprises a switching circuit (resistive load inverter) (See Fig. 1, items SW1-SW2) and wave-shaping circuit (inverter) (See Fig. 1, items SW3, 6, Col. 7, Lines 47-65).

It would have been obvious to one ordinary skill in the art at the time of invention to incorporate teachings of Kusumoto et al. into Willis et al. and McKnight system in order to increase accuracy of voltage comparison (See Col. 5, Lines 43-47 in Kusumoto et al. reference).

Allowable Subject Matter

5. Claims 38,40-43,48-49,53,55,66 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 38 the major difference between the teaching of the prior art of record (McKnight, Willis et al.) and the instant invention is that the resistive load inverter has a first and a second supply connection for connecting to lower supply voltage and a higher supply voltage respectively, wherein any of the first or second supply connection are connected to a sloping voltage source.

Relative to claim 40 the major difference between the teaching of the prior art of record (McKnight, Willis et al.) and the instant invention is that the comparator device comprises a shunting resistive device and an inverter.

Claims 41-43 depend on claim 40.

Relative to claim 48 the major difference between the teaching of the prior art of record (McKnight, Willis et al.) and the instant invention is that the mirroring circuit comprises a first switch element having a first and a second data electrode and a control electrode, the first switch element being connected with its first data electrode to

an electrode of the first memory element and with its second data electrode to the first pixel electrode, a second memory element for storing data values, the second memory element having a first and a second electrode, the second memory element being connected with its first electrode to the second data electrode of the first switch element, and with its second electrode to the control electrode of the first switch element, and resetting means, for resetting the data value stored in the second memory element.

Claim 53 depend on claim 48.

Relative to claim 49 the major difference between the teaching of the prior art of record (McKnight, Willis et al.) and the instant invention is that a second switch element between the first memory element and a data line for providing pixel data values.

Claim 55 depend on claim 49.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
10.02.07

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